STUDY MODULE DESCRIPTION FORM

Name of the module/subject **Programmable digital systems**			Code **1010812121010841101**
Field of study **Electronics and Telecommunications**	Profile of study (general academic, practical) **general academic**		Year /Semester **1 / 2**
Elective path/specialty **Radio Communications**	Subject offered in: **Polish**		Course (compulsory, elective) **obligatory**
Cycle of study: **Second-cycle studies**	Form of study (full-time,part-time) **full-time**		
No. of hours Lecture: **1** Classes: **-** Laboratory: **2** Project/seminars: **-**			No. of credits **4**
Status of the course in the study program (Basic, major, other) **other**	(university-wide, from another field) **from field**		
Education areas and fields of science and art **technical sciences**			ECTS distribution (number and %) **4 100%**

Responsible for subject / lecturer:

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Prerequisites in terms of knowledge, skills and social competencies:

1	**Knowledge**	1. Has a basic knowledge of Boolean algebra. 2. Has knowledge in area of programming in C/C++. 3. Has a general knowledge about combinational and sequential digital circuits. 4. Has a general knowledge in area of binary arithmetic and digital representation of signals.
2	**Skills**	1. Is able to look for information required during design process and take educational courses, if needed, especially through Internet and distance education.
3	**Social competencies**	1. Knows the limitations of their own knowledge and skills; can precisely formulate questions; understands the need for further education and systematic reading of scietnific journals in the field. 2. Can work individually and in team; knows the responsibility for tasked realized in team.

Assumptions and objectives of the course:

The main purpose of the course is to show various design technics for digital systems that can be suitable for FPGA devices. As hardware description language the Verilog will be used. A lot of examples will show how to efficiently use all basic and generic FPGA blocks (like RAM, DSP, etc.).

Laboratory work will be performed with exploiting XILINX FPGA boards.

Study outcomes and reference to the educational results for a field of study

Knowledge:

1. Student has a basic skill in design of simple digital devices - [K2_W01,K2_W02]
2. Student has a basic knowledge about the principle of operation of fast communication interfaces - [K2_W01,K2_W02]
3. Student has a basic knowledge about designing a state machines - [K2_W01,K2_W02]

Skills:

1. Can describe complex digital system as a hierarchy of modules using Verilog language - [K2_U04]
2. Can correctly determine the parameters of the interface between the two frequency domains - [K2_U04,K2_U12]
3. Can acquire data from the literature and other sources, can integrate the information, make their interpretation, as well as formulate and to justify opinions - [K2_U01]

Social competencies:

1. Can see and analyze development of design techniques - [K2_K04]
2. Ability of self-learning (textbooks, computer programs) - [K2_K05]
3. Knowing the responsibility for the electronic and telecommunication systems being designed - [K2_K06]

Assessment methods of study outcomes
Individual projects, written exam.

Course description
Introduction to digital programmable devices. FPGA devices (especially XILINX and ALTERA devices). Basic embedded blocks (RAM, PLL, FIFO, etc.) Inter-domain communication (source-synchronous interface). System-onChip (SoC). Communication s interfacesand buses (AMBA, CoreConnect, etc.). Network-on-Chip (NoC). Design and synthesis methods for FPGA devices.

Basic bibliography:

1. Łuba T. (red.), Rawski M., Tomaszewicz P., Zbierzchowski B.: Synteza układów cyfrowych, Wydawnictwa Komunikacji i Łączności, Warszawa 2003
2. Hajduk Z.: Wprowadzenie do języka Verilog, BTC, Warszawa 2009.
3. Synteza i optymalizacja układów cyfrowych, Giovanni De Micheli, WNT.
4. Język VHDL, Kelvin Skahill, WNT.
5. Synteza i analiza układów cyfrowych, Autor: Halina Kamionka-Mikuła, Hanryk Małysiak, Bolesław Pochopień, WKŁ.

Additional bibliography:

1. Zbysiński P., Pasierbiński J.: Układy programowalne pierwsze kroki, Wydawnictwo BTC, Warszawa 2004,
2. Łuba T.. : Synteza układów logicznych. Oficyna Wyd. PW, Warszawa, 2005.

Result of average student's workload

Activity	**Time (working hours)**
1. Activities that require personal contact with an academic teacher	20
2. Reading literature (manuals, directories)	15
3. Preparation for the lab	10
4. Preparation for the exam	10

Student's workload

Source of workload	**hours**	**ECTS**
Total workload	100	4
Contact hours	50	1
Practical activities	65	3